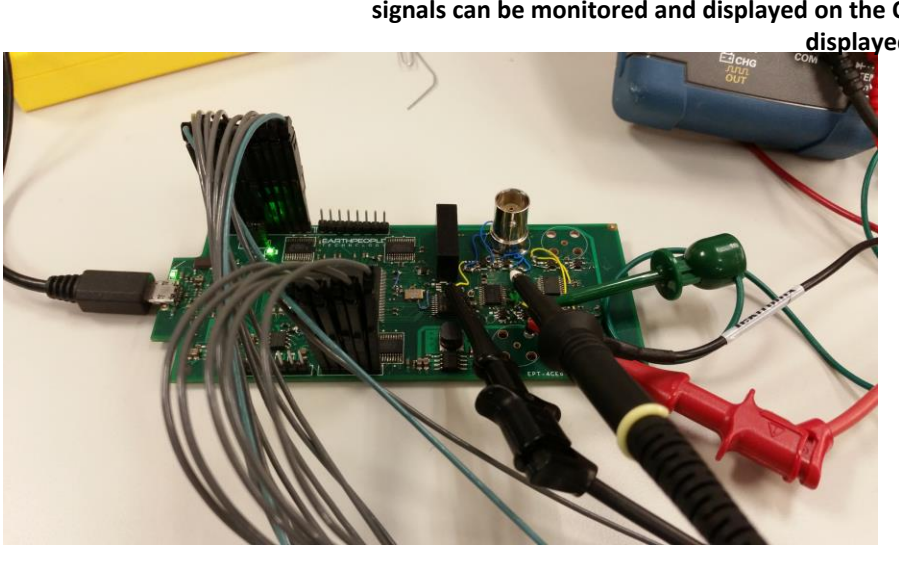
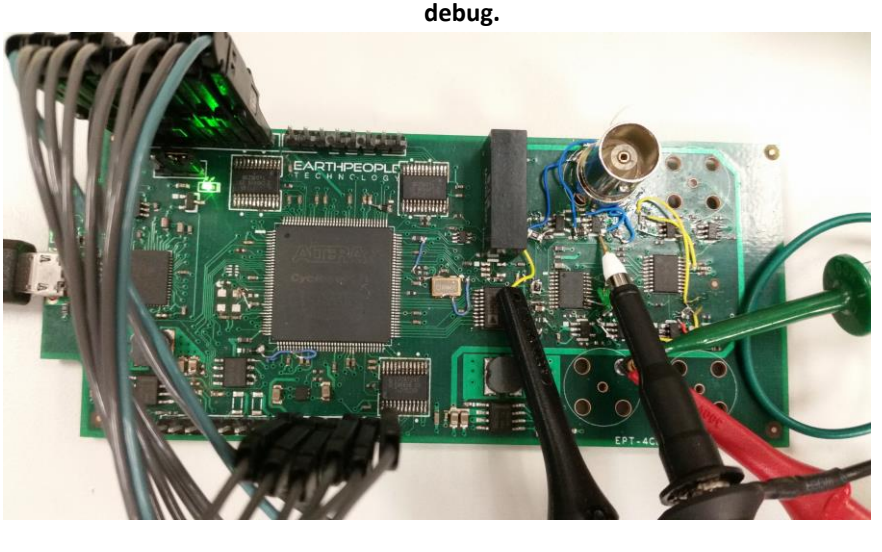
EPT OSCILLOSCOPE INTERFACE BOARD DEVELOPMENT

Debugging the EPT DSO V1 board has been performed using a Mixed Signal Oscilloscope. 16 digital signals can be monitored and displayed on the Oscilloscope. Also four channels of analog can be displayed as well.



Single Board PCB with 24 I/O pins broken out to connectors for connections to DSO.

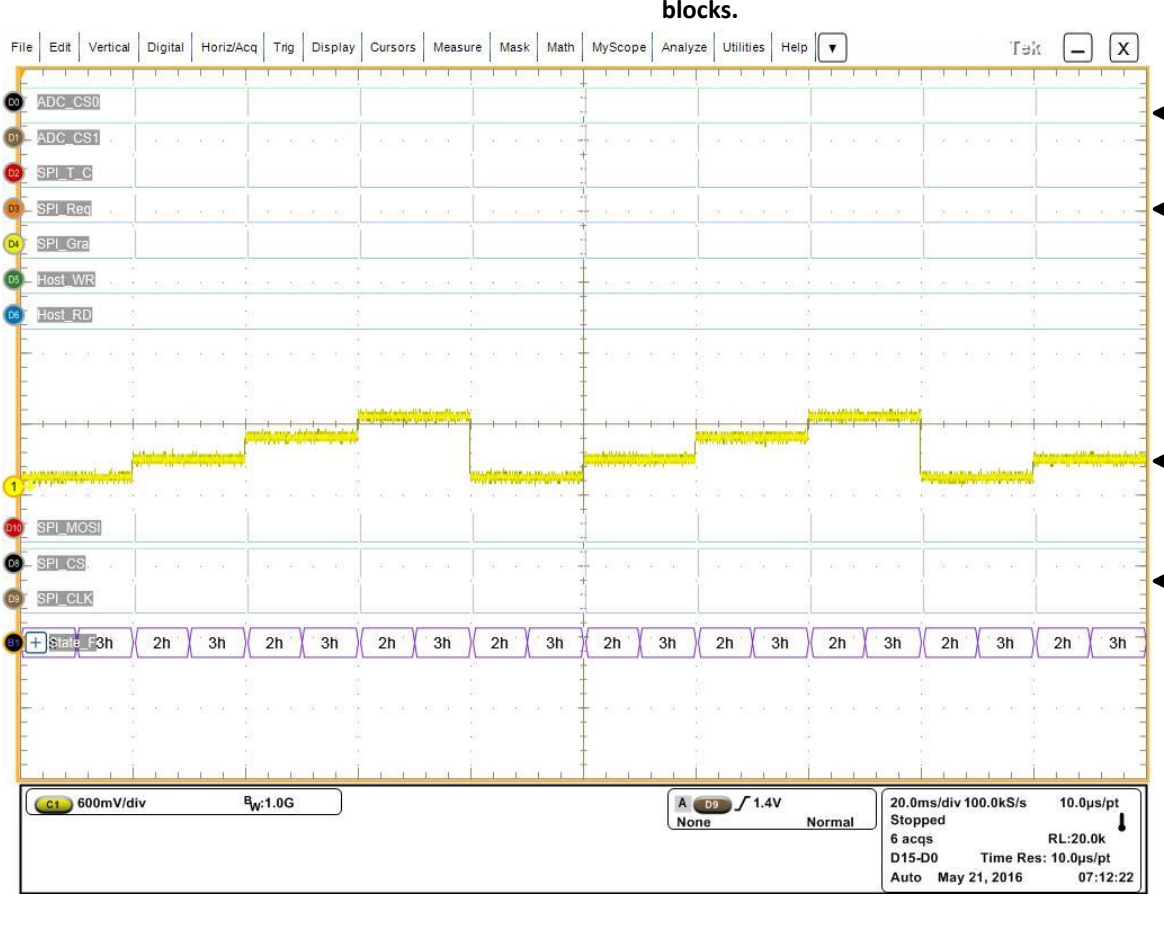
There has been many cut traces and jumper wires added to the EPT DSO during debug.



Probing the EPT Oscilloscope Int Board with Logic Analyzer and Oscilloscope to examine signals in real time.

Internal FPGA signals are connected to FPGA pins which allows these signals to be displayed on the Oscilloscope.

This screen shot from the Oscilloscope shows the FPGA internal signals communicating with Memory and SPI blocks.



ADC State Machine Controller

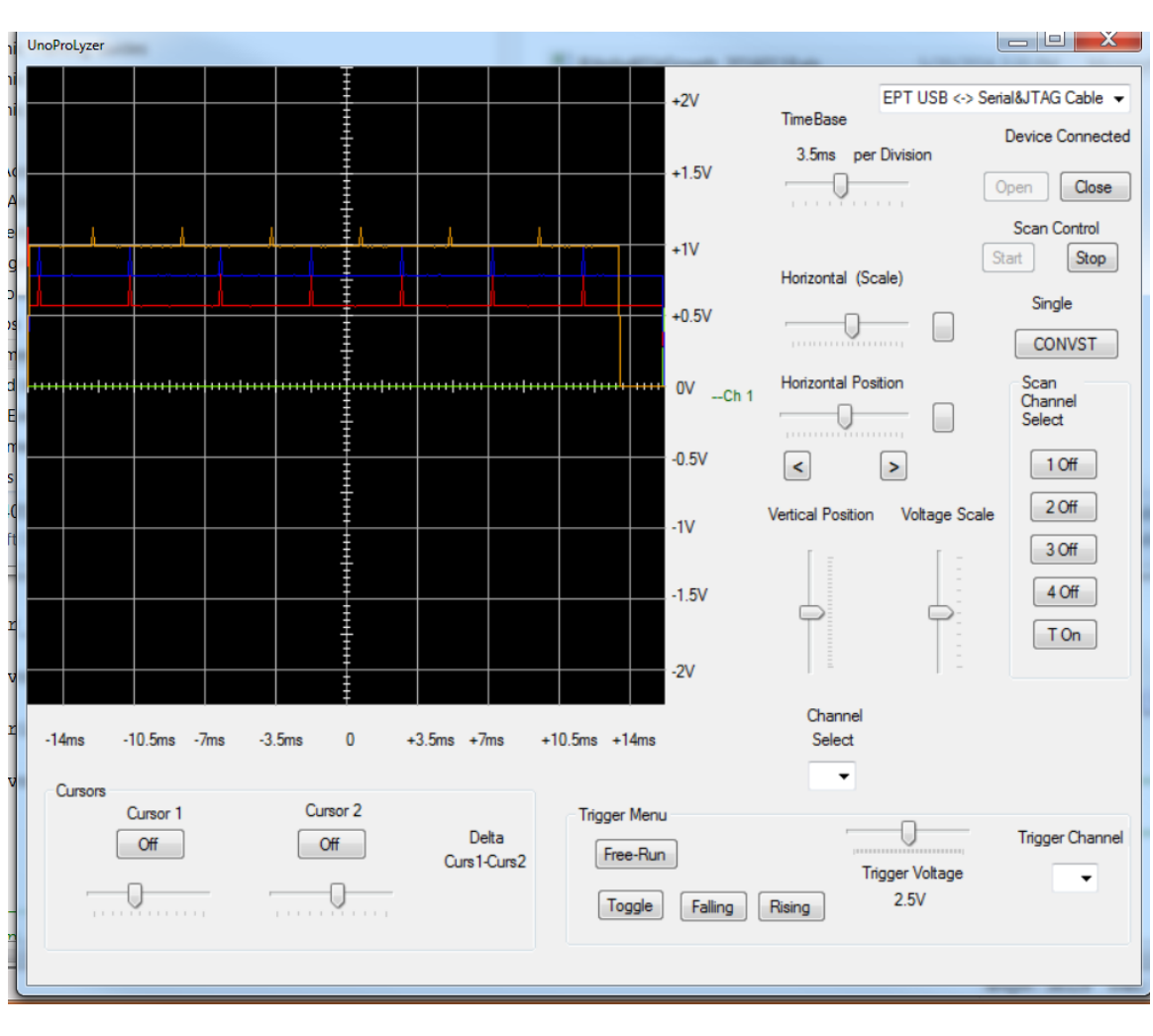
Internal Memory Bus Grant/Request

Oscilloscope Measurement of signal applied to the ADC

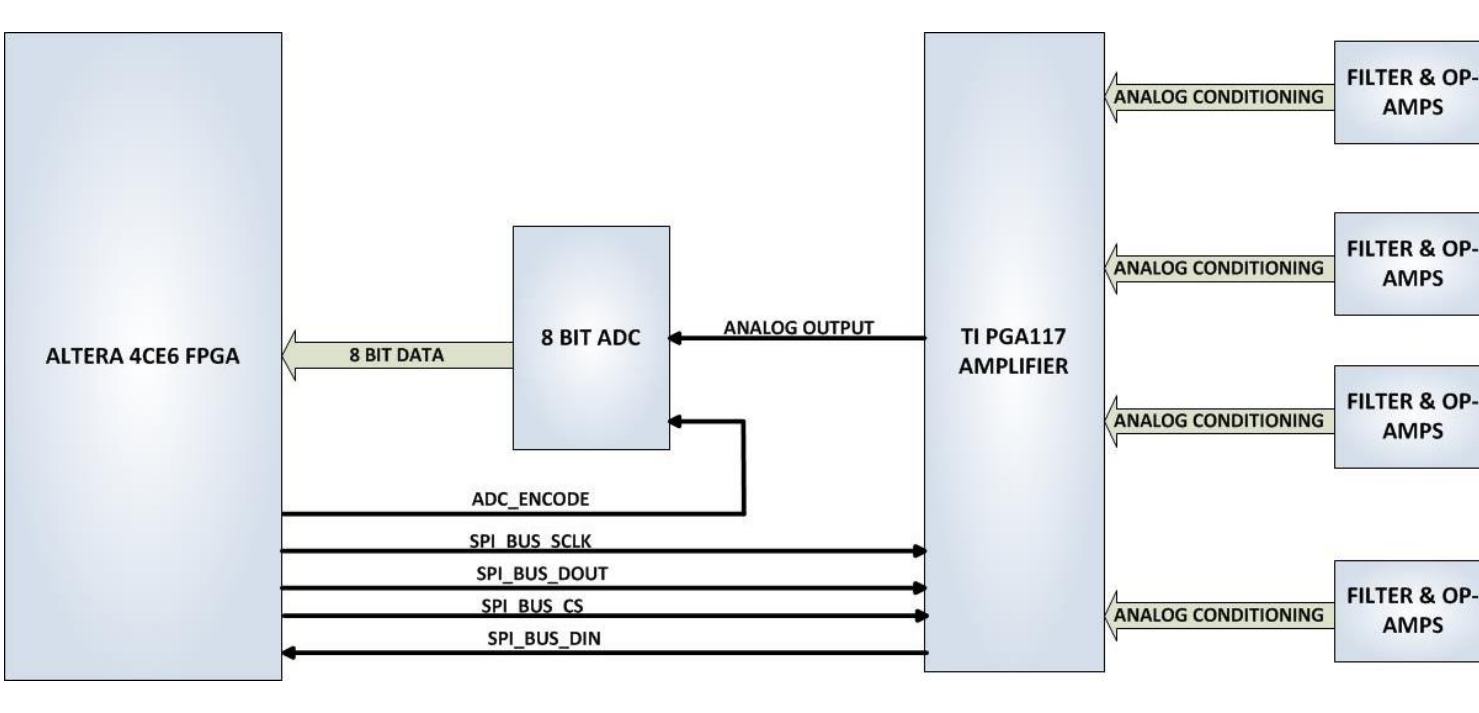
External SPI Bus to PGA

FPGA Code is initiated by the UnoProLyzer Software. This software is also used to capture and display signals from the ADC.

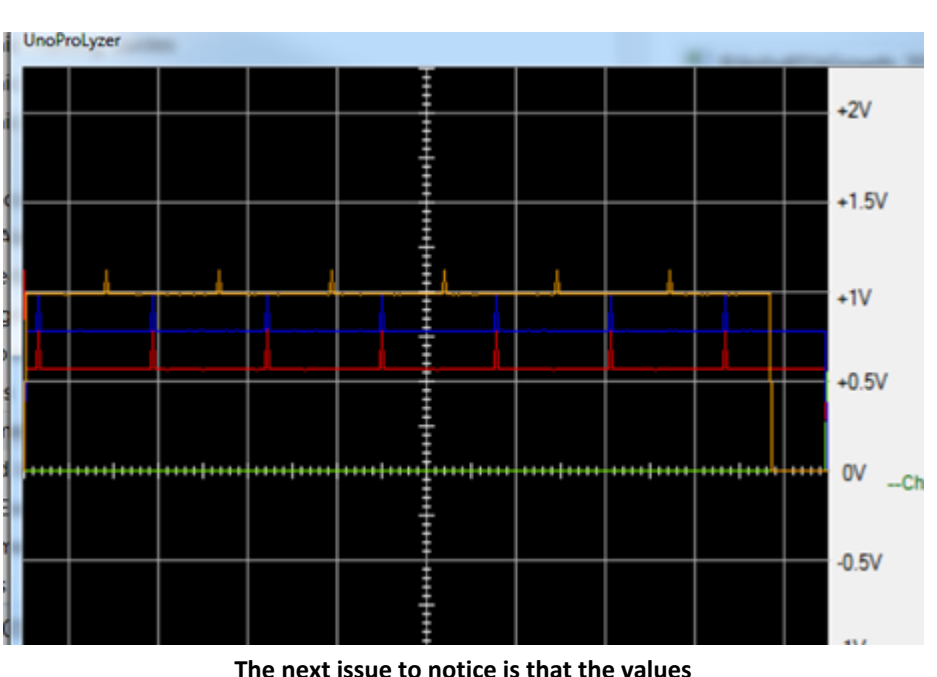
This is a screen shot from the UnoProLyzer Software. This shows the four channels being populated with data from ADC.



The FPGA is correctly cycling through all four channels and storing the results of the ADC conversion correctly in its local memory.



This verifies that the PGA and FPGA channel switching is occurring correctly. The issues that can be seen are the "glitches" (positive going pulses) that occur every few milliseconds. The height of these pulses does not seem to be correlated to fixed value. These will have to be investigated further.



Four analog channels are displayed as:

- **Channel 1 = 0V**
- **Channel 2 = 0.6V**
- **Channel 3 = 0.8V**
- **Channel 4 = 1.0V**

The next issue to notice is that the values are 0V, 0.6V, 0.8V and 1.0V.

The EPT DSO board has fixed voltage dividers providing a test voltage for each of the four channels. From the oscilloscope screen shot, it can be seen that

- **Channel 1 = 100mV**
- **Channel 2 = 200mV**
- **Channel 3 = 400mV**
- **Channel 4 = 600mV**

The ADC converts these positive values into the upper half of the eight bit range of values. The ADC uses a reference voltage of 1.2V peak to peak. This means the Maximum Positive Voltage the ADC will correctly convert is 0.6V.

FUNCTIONAL BLOCK DIAGRAM

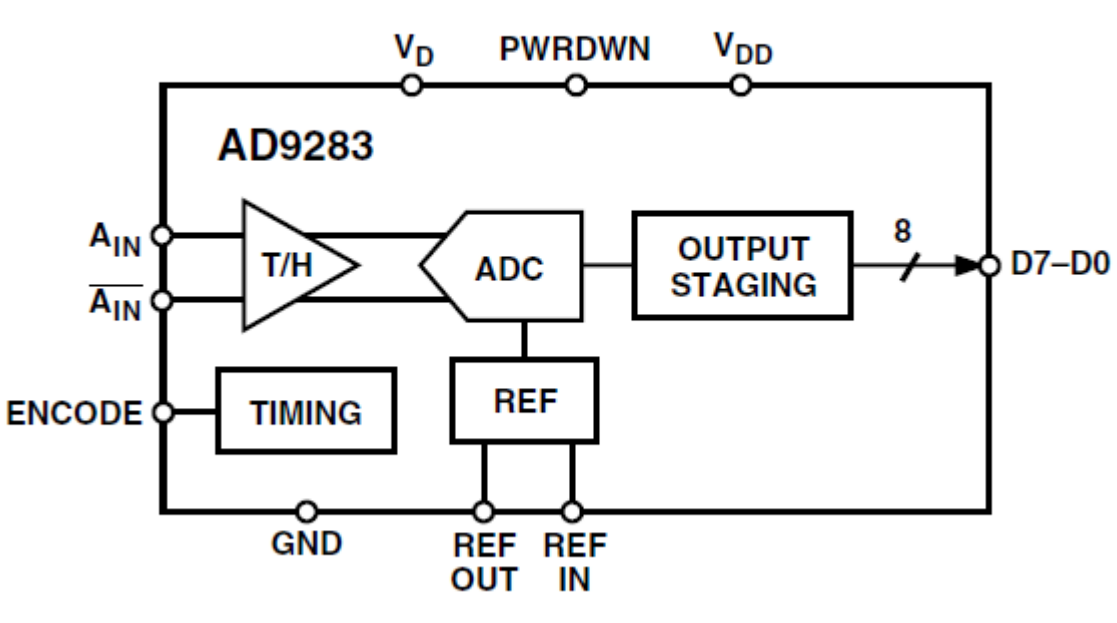


Table I. Output Coding (VREF = 1.25 V)

Step	$A_{IN}-\overline{A_{IN}}$	Digital Output
255	0.512	1111 1111
•	•	•
•	•	•
128	0.002	1000 0000
127	–0.002	0111 1111
•	•	•
•	•	•
0	–0.512	0000 0000

So, the positive range of the ADC means that:

0.0V = 128 counts from the ADC
0.6V = 256 counts from the ADC

For the negative range on the ADC:

-0.6V = 0 counts from the ADC

```
        n = StorageArray[xpos];
    else
        StorageArray[xpos] = n;

    // n between 0 and 1023
    //System.Single y = 0;
    //System.Single volt = 0;
    int yint = 0;

   //Scaling to be used on the incoming data
   int BitScale = 1024;


    //Scale the data words to 16 bits
    double Data;
    Data = (double)((n * 450) / BitScale);

    n = (int)Data;
    //ymax = 256;
    ymax = 225;

    // scale the voltage according to the voltage scale control
```

The UnoProLyzer Software is set up for values from a 10 But ADC (the UnoProLogic2). This can be seen from the above code snippet with multiplying the sample "n" by 450 (This gives an offset of 450 pixels from the top most pixel. The resulting conditioned value will be subtracted from the bottom most pixel value before displaying the pixel value. This is a method to place the pixel correctly in the oscilloscope window). Then dividing by the total number of counts per ADC range (the old value of 1024 counts has not been changed from the UnoProLogic2's 10 bit ADC). This value should be 256.

So, a value of 128 will be displayed as 0.5V on the UnoProLyzer Oscilloscope window. The positive deflections from 128 will be displayed as increments from +0.5V up to +1.0Von the UnoProLyzer Oscilloscope window. This will be fixed in the next release of software.

Next issue to notice is the ADC is a true bipolar input. This means for the positive range of the ADC:

0.0V = 128 counts from the ADC
0.6V = 256 counts from the ADC

For the negative range on the ADC:

-0.6V = 0 counts from the ADC

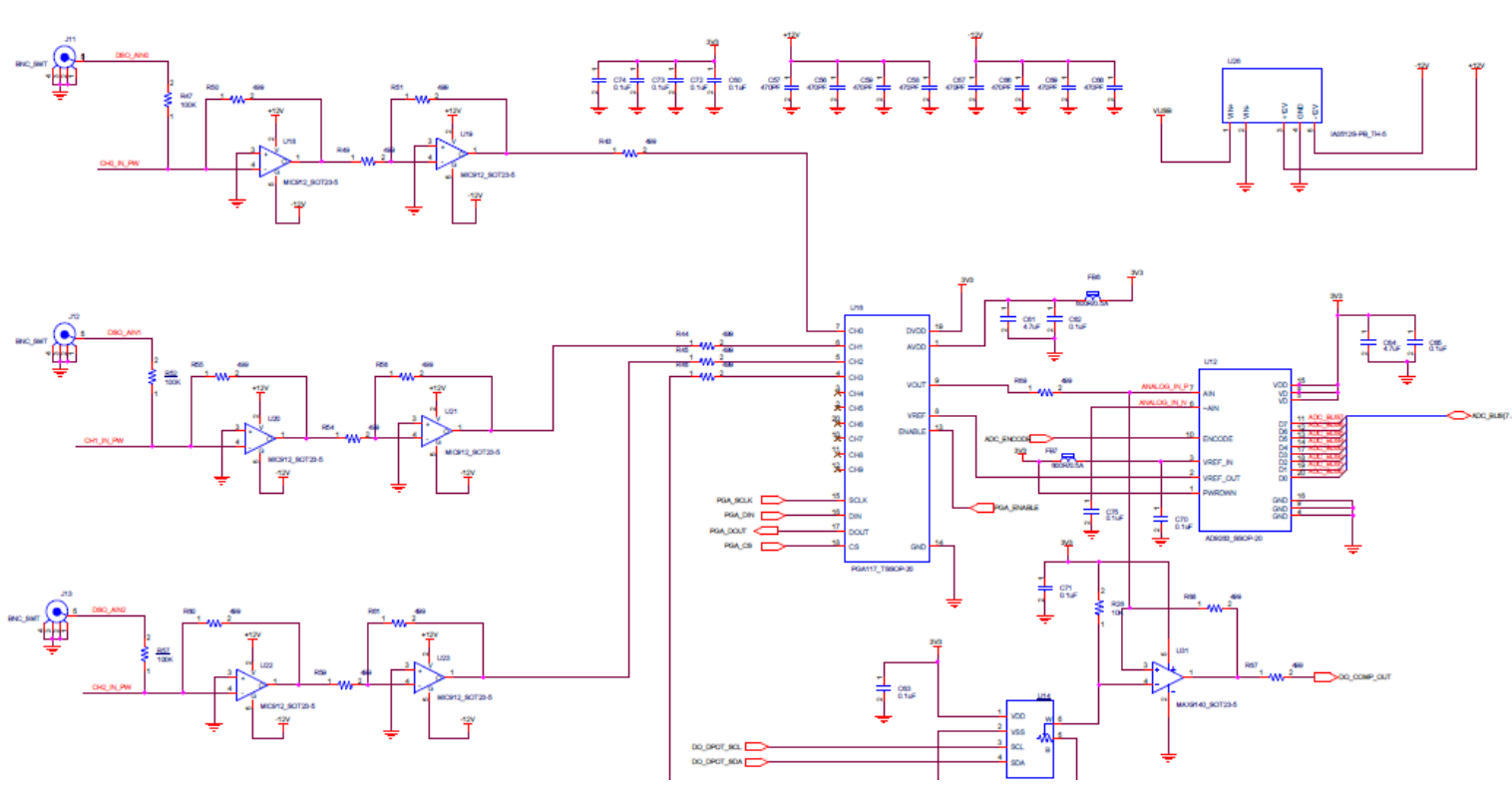
ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range, unless otherwise noted.

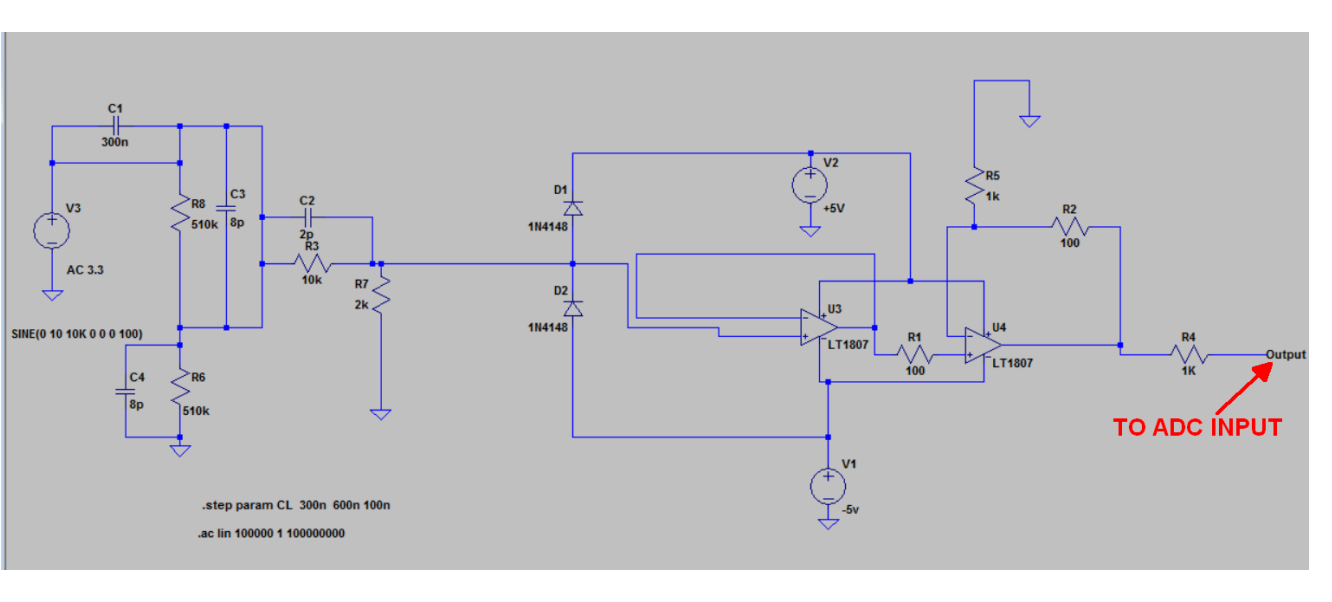
		PGA112, PGA113, PGA116, PGA117	UNIT
Supply Voltage		+7	V
Signal Input Terminals, Voltage[2]		GND – 0.5 to (AV_{DD}) + 0.5	V
Signal Input Terminals, Current[2]		±10	mA
Output Short-Circuit		Continuous	
Operating Temperature		–40 to +125	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		+150	°C
ESD Ratings:	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	300	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may

This is a problem because the PGA117 part is unipolar only. It only accepts and outputs signal from 0V to AVDD. So, this analog front end will never correctly display the output of the Op-Amp signal conditioners.

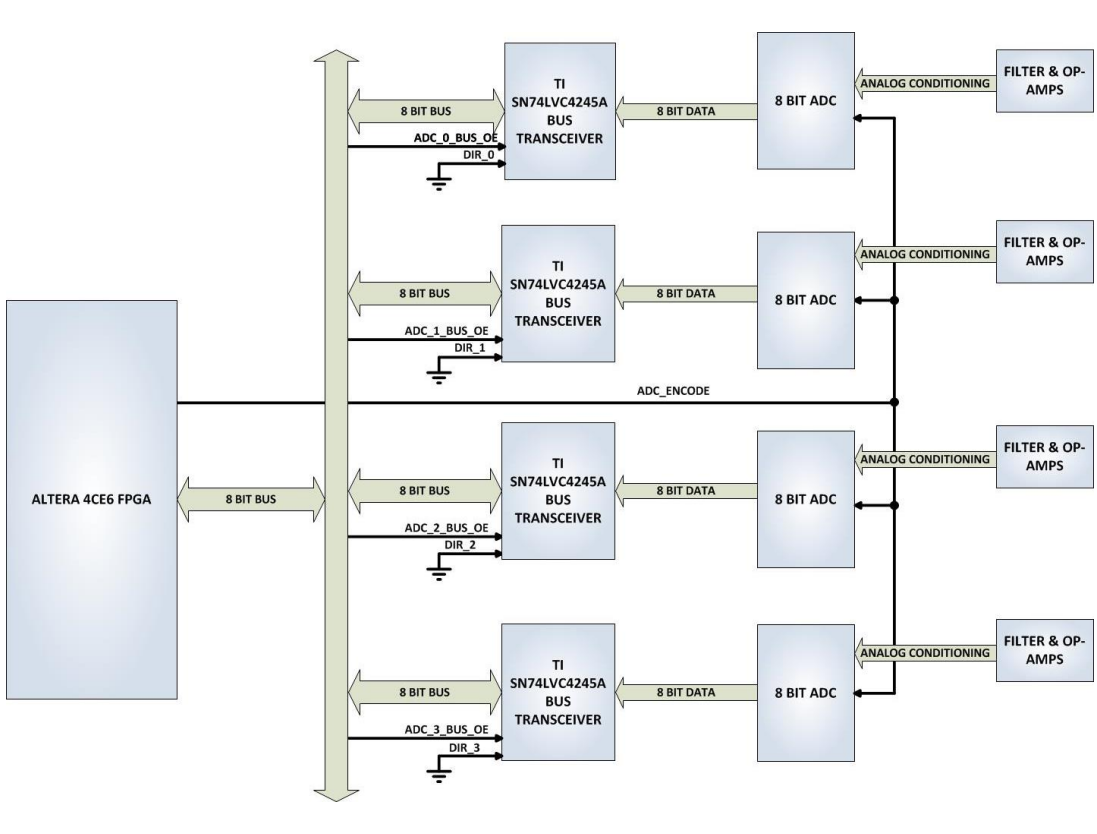


The analog front end circuit must be changed to remove the PGA117 and redesign the Op-Amp circuit to the above circuit. The output of this circuit will feed directly into the ADC. This circuit was simulated and correctly output the +/- 40 volts down-converted to +/-0.6 volts.



Redesigning the circuit to remove the PGA117 part will eliminate the ability of the circuit to select a single channel for input into the ADC. So, we need a hardware switching mechanism to select a channel.

After searching through several analog multiplexor parts, it was determined that there is not a good cheap part to accomplish this switching at the analog signal level.



So, it was determined that four separate 8 Bit High Speed ADC's would be used with their output buses tied to 8 bit transceivers. The output of the transceivers will be connected to one eight bit bus that is connected to the FPGA.

This scheme will allow the FPGA to select a channel by turning on the Output Enable signal of the selected channel. The multiplexing is done at the digital level.

This approach of using four separate 8 Bit ADCs will increase the cost of the overall board. However, the benefits are true 80MSamples per Second for each channel. So, each channel will have a bandwidth of 10-15MHz.

Besides the increased cost of the board, the size of the board will grow to accommodate the extra IC's. The new schematic and layout are complete. The design and layout are being reviewed at this time. The new layout is below.